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NEW ACTIVE BODY BIASED DOIND-ABC2 FOR HIGH SPEED DOMINO LOGIC AT 70NM NODE TECHNOLOGY

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ABSTRACT

In the resent VLSI technology high speed devices are used in much application, such as dynamic logic circuits because it is give the best performances over the static device due to less delay, less noise immunity and low power dissipation. Increase Leakage current combine with noise immunity it degrade the performance of dynamic logic circuit.

In this paper body biased DOIND-ABC2 (DOIND-2) logic is proposed to reduce the leakage current with less delay penalty. In this paper different Active body biased technique for DOIND logic approach namely DOIND-2(ABC-2) has been used to analyze different parameters Proposed DOIND-2 approach has maximum 70% improvement in leakage current among Domino, DOIND and DOIND-1 proposed technique as compare to domino logic circuit. Proposed DOIND-2 approach also has improvement in most of parameter as compare to all other approaches .In this paper effect of frequency variation in different circuits has been analyzed. All the parameter has been performed at 70 nm technology node using tanner EDA tool with supply voltage 0.9v.

KEYWORDS: Precharge, power dissipation, active body biased, Domino logic, valuation, DOIND-2.

INTRODUCTION

In the VLSI industry has challenges to limits of traditional silicon CMOS scaling; the introduction of performance boosters such as novel materials and innovative device structures has become necessary for the future of CMOS scaling [2].

To improve the performance of portable systems and less power consumption in very high density VLSI chips result in quick and inventive growth of low power design. Higher power decay reduces the Battery life in battery operated applications and also reduces the reliability. The leakage Current increases drastically with each new technology inventions. In deep-submicron technologies Leakage power loss is a major problem because it drains the battery even when a system (Circuit) is completely idle. As scaling down the technology node, power supply and threshold voltage also roll down because power supply voltage and threshold voltage of MOS transistor is critical parameters to regulate the performance and switching speed of MOS devices.[3]

In this paper domino logic Active Body Biased DOIND-ABC2 (DOIND-2) Approach is used to analyze different parameter.

RELATED WORK

VLSI technology uses different techniques presented to control leakage current in domino logic circuits. There are presented some technique that is control the leakage current.

In the Lector Technique [4] two leakages control transistor (one PMOS and one NMOS) is introduce between pull-up and pull-down circuits within standard logic circuits. This arrangement ensures that one of the LCTs always operates in its near cut off region .the basic idea behind LECTOR approach is that “a state with more than one transistor OFF in a path from supply voltage to ground.

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INDEP approach [5] is the technique to reduce the leakage current in nanoscale circuit. In this approach to extra inserted transistors between pull up and pull down networks that are input logic dependent.

DOIND approach [6] In the DOIND (**Do**mino logic with Clock and **IN**put **D**ependent transistors) logic circuit. It has two DOIND transistors MP4 (PMOS) and MN4 (NMOS) connected between A and B. Gate terminal of DOIND transistors (MP4 and MN4) are V0 and V1 which are clock and input logic dependent respectively

PROPOSED WORK

Adopting body biasing DOIND logic

In this paper we proposed DOINDAB (**Do**mino logic with Clock and **IN**put **D**ependent transistor with **A**ctive **B**ody Biasing) ABC2. For the static circuit's body of SOI partially Depleted MOSFET biased to control the threshold dynamically.

DOIND-2 (ABC-2) Technique

A proposed DOIND-2 logic circuit is shown in fig.1.1. It has two DOIND transistors MP4 (PMOS) and MN4 (NMOS) connected between A and B. Gate terminal of DOIND transistors (MP4 and MN4) are V0 and V1 which are clock and input logic dependent respectively. Body biasing MP5 (PMOS) has placed in the transistor MP4 (PMOS). Gate terminal of PMOS transistor MP5 connected to the gate terminal of PMOS transistor MP4, Source terminal of PMOS transistor MP5 connected to the point A of PMOS transistor MP1 and MP4. Drain terminal of PMOS transistor MP5 connected to the Body of the PMOS transistor MP4. Body Biasing MN5 (NMOS) set to the Transistor MN4 (CMOS).

NMOS transistor MN5 biased with the NMOS transistor MN4. Gate terminal of NMOS transistor connected to the gate termina1 of the NMOS transistor MN4 and source to the Body terminal of the NMOS transistor MN4 and drain terminal connected point B of the NMOS transistor MN2 and MN4 Body terminal of all PMOS transistors are connected to Vdd and Body terminal of all NMOS transistors are connected to Gnd.

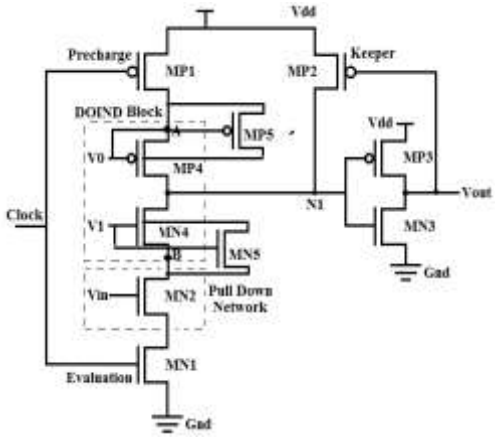

Fig: 1.1: DOIND-2 Logic circuit

The working operation of DOIND-2 logic circuit is in the following manner .When the clock signal is low, and then V0 should be 0 (low) so that MP1, MP4 and MP5 is turn on and the DOIND logic circuit comes in precharge phase. During precharge phase, the node N1 is charged to Vdd through MP1, MP4 and MP5. Vout of the circuit is low which turn on the keeper transistor (MP2). When the clock signal is high, the circuit enters into the evaluation phase. In evaluation phase, when input Vin = 1 (high) then V1 should be 1 so that dynamic node N1 becomes 0 and when input Vin = 0 (low) then V1 should be 0 so that dynamic node N1 becomes 1.

Different parameter analysis of Adaptive Body biased DOIND approach

In this section the TSPICE simulator is used for study Of DOMINO logic based buffer with different clock frequency. All the experimental data were obtained at 70nm technology node. Channel width 270ns and channel length are same for NMOS transistors which are equal to technology node and channel width of all PMOS is 2X of channel length except keeper transistor. Channel length of keeper transistor is 5X and width is 2X of technology node. Vdd power supply is 0.9 v taken for the simulation.

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As delay and leakage current of the circuit is a function of clock pulse, input value and logic circuits

Impact on Leakage Current:

Relation between leakage current and threshold voltage is given by [6],

$$I_{Leakage} = I_0 \frac{(Vgs-Vth)}{\eta Vt} (1\text{-}\exp \frac{-Vds}{Vt})$$

Where Vgs is gate to source voltage; I_0 is saturation current, and η is subthreshold slope factor and V_t is drain to source voltage.

Table:1: Leakage current at different clock pulse.

logic design	Clk=0, Vin=0	Clk=0, Vin=1	Clk=1 Vin=0	Clk=1, Vin=1	Improv In %
Domino	0.307	1.595	2.262	2.126	
DOIND	0.160	0.307	0.127	0.258	86%
DOIND-B	0.166	0.322	0.322	0.264	83%
DOIND-1	0.160	0.307	0.306	0.259	84%
DOIND-2	0.175	0.358	1.091	0.278	70%

DOIND -2 have 70% better improve than the Standard Domino logic but DOIND indicate the best result 86% improvement than other comparative logic circuits.

At the clock $=V_1=V_{IN}=0$ show the lower leakage current at all the logic circuits but when we apply clock $=V_1=V_{IN}=1$ all the logic have higher leakage current.

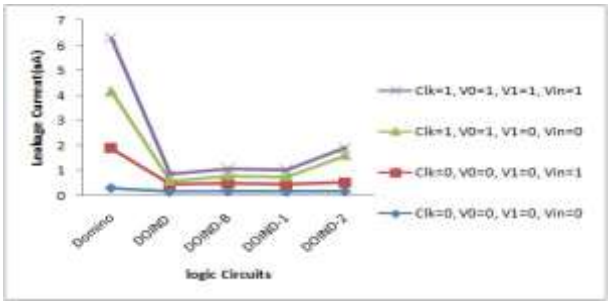

Fig.1.2 Leakage current in (nJ)

Impact on Static Power:

Static Power defined by the given formula.

Static Power = Leakage Current*Vdd, Where Vdd is the power supply of the logic Circuits.

logic design	Clk=0 Vin=0	Clk=0 Vin=1	Clk=1Vin=0	Clk=1 Vin=1	% improv
Domino	0.276	1.435	2.036	1.913	
DOIND	0.144	0.276	0.115	0.232	86%
DOIND-B	0.149	0.290	0.290	0.237	83%
DOIND-1	0.144	0.276	0.276	0.233	84%
DOIND-2	0.157	0.322	0.982	0.250	70%

Table2: Impact on Static Power

From the above table DOIND, 86% improvement than domino logic circuit But DOIND-2 have also 70% better than the Domino Logic circuit.

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Impact on Static Energy:

Static energy element is directly proportional to Vdd so static energy is represented as

$$E_{Static} = I_{Leakage} V_{dd} T_{delay}$$

Where $I_{Leakage}$ is leakage current and T_{delay} is circuit delay.

Table: 3: Static Energy at different clock frequency

logic design	At 50MHz	Gain	At 5MHz	Gain
Domino	92.971		158.10	
DOIND	19.132	79%	19.709	88%
DOIND-B	36.400	61%	33.408	79%
DOIND-1	57.194	38%	2.5085	98%
DOIND-2	39.807	57%	65.125	59%
logic design	At 500kHz	Gain	At 50kHz	Gain
Domino	158.1		155.70	
DOIND	20.08	87%	20.094	87%
DOIND-B	30.78	81%	30.880	80%
DOIND-1	2.478	98%	4.653	97%
DOIND-2	59.98	62%	58.26	63%

At the higher frequency Static Energy Gain is lower but it is better than Domino Logic , its 57%, 59%, 62% and 63 % improvement . Table shows when we decrease the Clock frequency its give the best improvement

Impact on Static PDP

Static energy delay product (EDP) and Static power delay product (PDP) is given by

$$EDP_{static} = E_{static} \times T_{delay}$$

$$PDP_{static} = P_{static} \times T_{delay}$$

Table 4.5.3 shows various logic circuits and there value of static PDP with different clock frequency.

Table: 4.: Static PDP on different clock periods

Logic design	50MHZ	% impro	5MHZ	% impro
Domino	92.97		158.1068	
DOIND	19.13	79%	19.70967	88%
DOIND-B	33.36	64%	33.40882	79%
DOIND-1	62.64	33%	2.747437	98%
DOIND-2	39.80	57%	65.12519	59%
Logic design	500KHZ	% impro v	50MHZ	% impro v
Domino	158.10		155.7074	
DOIND	20.075	87%	20.09425	87%
DOIND-B	30.780	81%	30.88084	80%
DOIND-1	2.7143	98%	5.097285	97%
DOIND-2	59.979	62%	58.26607	63%

Static PDP again show the approximate same improvement than Domino Logic circuit. When we increase the clock frequency its decrease the improvement

Impact on Dynamic power:

Dynamic power is **power** consumed while the inputs are active. When inputs have ac activity, capacitances are charging and discharging and the **power** increases as a result. The dynamic power includes both the ac component as well as the static component.

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Table: 5: Dynamic Power at different frequency

Logic design	50MHZ	% improve	5MHZ	% improv
Domino	63.10273		63.10273	
DOIND.	151.7647	-141%	17.3993	72%
DOIND-B	64.24351	-181%	8.995963	86%
DOIND-1	82.51929	-31%	49.50935	22%
DOIND-2	90.62208	-44%	9.847387	84%
Logic design	500KHZ	% improve	50KHZ	% improv
Domino	0.111690		0.11	
DOIND.	3.702617	-3215%	2.493134	-2166%
DOIND-B	4.287091	-3738%	61.87233	-5614%
DOIND-1	3.004553	-2590%	2.423472	-2103%
DOIND-2	3.189672	-2756%	2.461738	-2138%

Table indicate that clock Frequency 50MHz , 500KHz and 50KHz Dynamic Power has Drawbacks but at the clock frequency 5MHz have DOIND, DOIND-B, DOIND-1and DOIND-2(ABC2) show 72%, 86%, 22% and 84% improvement Than Domino Logic circuit.

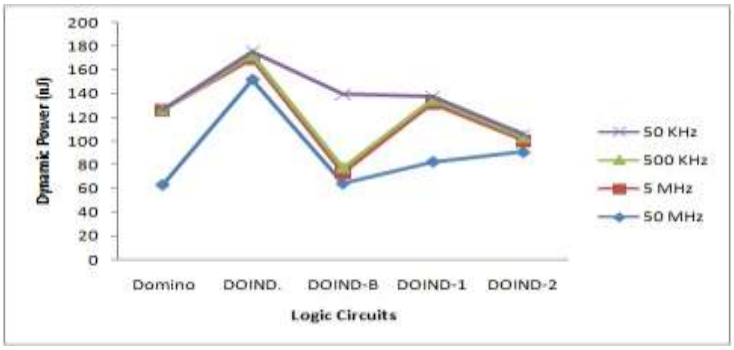

Fig.1.4: Dynamic Power (nJ)

Impact on Delay:

In most designs there will be many logic paths that do not require any conscious effort when it comes to speed. However, usually there will be a number of paths, called the critical paths that require attention to timing details. These can be recognized by experience or timing simulation, but most designers use a timing analyzer, which is a design tool that automatically finds the slowest paths in a logic design.

Table; 6: Delay at different clock period

Logic design	500KHZ	% improv	50KHZ	% improve
Domino	111.6905		110	
DOIND.	104.4	7%	104.5	5%
DOIND-B	127.1756	-14%	127.59	-16%
DOIND-1	10.65	90%	20	82%
DOIND-2	140	-25%	136	-24%

DOIND-2 show here drawbacks But DOIND and DOIND-1clear show the 8% and 90% improvement than Domino logic circuit.

Table; 7: Delay at different clock period

Logic design	50MHZ	% improv	5MHZ	% improve
Domino	65.68		111.69	

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DOIND.	99.5	-51%	102.5	8%
DOIND-B	137.87	-110%	138.03	-24%
DOIND-1	245.78	-274%	10.78	90%
DOIND-2	151.06	-130%	152.01	-36%

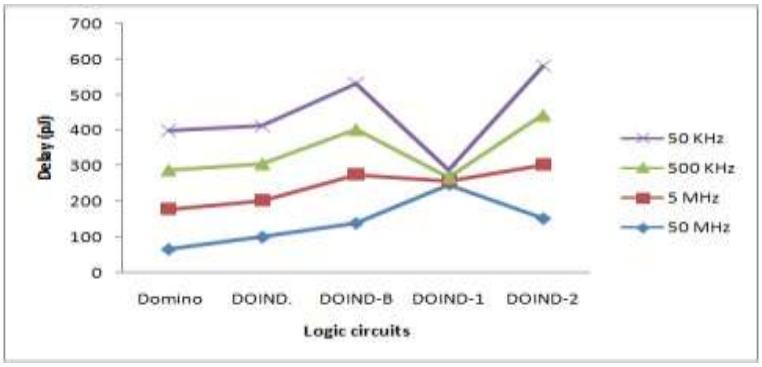

Fig.1.5: Delay in (pJ)

Impact on Dynamic PDP:

In the table shows that DOIND-2 have a 79% better improve than Domino Logic at the 5MHZ frequency and 500KHZ frequency and 50KHz frequency DOIND-2 Logic have a higher improvement approx. 92% and 95% than Domino logic but DOIND, DOIND-B and DOIND-1 also better than Domino logic circuits for these two clock frequency.

Table: 8: Dynamic PDP at different clock period

Logic design	**50MHZ**	**% improv**	**5MHZ**	**% improve**
Domino	4.144		7.0482	
DOIND.	15.10	-264%	1.7834	75%
DOIND-B	8.857	-114%	1.2417	82%
DOIND-1	20.28	-389%	0.5337	92%
DOIND-2	13.68	-230%	1.4969	79%
Logic design	**500KHZ**	**% improve**	**50KHZ**	**% improve**
Domino	7.047		6.9413	
DOIND.	0.386	95%	0.2605	96%
DOIND-B	0.545	92%	7.8944	-14%
DOIND-1	0.031	100%	0.0484	99%
DOIND-2	0.446	94%	0.3347	95%

SIMULATION RESULT

IN this paper all the parameter are tested with the EDA tanner for domino logic, DOIND, DOIND-B , DOIND-1 and DOIND-2 approach with supply voltage 0.9V. In this section the TSPICE simulator is used for study Of DOMINO logic based buffer with different clock frequency. All the experimental data were obtained at 70nm technology node. Channel width= channel length =270ns are same for NMOS transistors and channel width of all PMOS is 2X of channel length except keeper transistor. Channel length of keeper transistor is 5X and width is 2X of technology node.

CONCLUSION AND FUTURE SCOPE

In VLSI design, Leakage power dissipation becomes major concern. Leakage current decreases the performance of battery of portable device. Even when the circuit is in idle mode and in reset mode. Unnecessary power

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consumption is held without operating the device. This chapter present the contribution of the work and future scope of the technology.

This paper work focus mainly towards different adoptive body biased technology for DOIND approach. Proposed DOIND-2 has average improvement in leakage current of 70% among all other circuits. All the circuits have been analyzed at four different clock frequency 50MHz, 5MHz, 500 KHz and 50 KHz respectively. Here we use the 70nm technology node for analysis the circuits but it can be different node technology may be applied.

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